CLAIM AMENDMENTS

Please amend the claims as described herein below.

1(**CURRENTLY AMENDED**). A method for forming a package device, comprising:

providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane;

attaching a tape to the package substrate along the first plane;

placing a first integrated circuit on the tape and in the cavity;

depositing encapsulating material over the first integrated circuit;

removing the tape;

placing a second integrated circuit adjacent to the first integrated circuit outside the cavity, wherein die attach material is interposed between the first integrated circuit and the second integrated circuit; and

depositing encapsulating material over the second integrated circuit.

2(**ORIGINAL**). The method of claim 1, wherein the package substrate further comprises first pads on the first surface and second pads on the second surface and first bond fingers on the first surface and second bond fingers on the second surface, further comprising;

electrically connecting the first integrated circuit to the first pads;

electrically connecting the second integrated circuit to the second pads; and

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads.

3(**CURRENTLY AMENDED**). A method of forming a package device, comprising;

providing a package substrate having a first side and a second side and having first pads on the first side and second pads on the second side;

placing a first integrated circuit on the first side and a second integrated circuit on a second side, wherein ~~no substrate~~ die attach material is interposed between the first integrated circuit and the second integrated circuit;

electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads; and

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads,

wherein at least one of the first pads is electrically independent of all of the second pads.

4(**ORIGINAL**). The method of claim 3, wherein the step of attaching is further characterized by:

the first integrated circuit being placed on the first side prior to the second integrated circuit being placed on the second side.

5(**ORIGINAL**). The method of claim 4, wherein the step of electrically connecting is further characterized by:

the first integrated circuit being electrically connected to the first pads prior to the second integrated circuit being electrically connected to the second pads.

6(**CURRENTLY AMENDED**). A method for forming a package device, comprising:

providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane;

placing a first integrated circuit in the cavity;

placing a second integrated circuit adjacent to the first integrated circuit outside the cavity, such that ~~no substrate~~ die attach material is interposed between the first integrated circuit and the second integrated circuit; and

depositing encapsulating material over the first integrated circuit and the second integrated circuit.

7(**ORIGINAL**). The method of claim 6, wherein the step of depositing comprises:

depositing a first portion of the encapsulating material over the first integrated circuit prior to the step of placing the second integrated circuit; and

depositing a second portion of the encapsulating material over the second integrated circuit.

8(**ORIGINAL**). The method of claim 7, further comprising:

placing a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material.

9(**ORIGINAL**). The method of claim 6, wherein the package substrate further comprises first pads on the first surface, second pads on the second surface, first bond fingers on the first surface, and second bond fingers on the second surface, further comprising;

electrically connecting the first integrated circuit to the first pads;

electrically connecting the second integrated circuit to the second pads; and

testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads.

10(**ORIGINAL**). The method of claim 9, wherein the step of electrically connecting the first integrated circuit comprises wire bonding.

11(**ORIGINAL**). The method of claim 6, wherein the package substrate further comprises a supporting member along the second plane of the substrate.

12(**ORIGINAL**). The method of claim 11, wherein the supporting member is between the first integrated circuit and the second integrated circuit.

13(**ORIGINAL**). The method of claim 12, wherein the supporting member is electrically conductive.

14(**ORIGINAL**). The method of claim 11, further comprising removing the supporting member prior to step of placing the second integrated circuit.

15(**ORIGINAL**). The method of claim 14, wherein supporting member is tape.

16(**WITHDRAWN**). A package device, comprising:

a package substrate having a first surface defining a first plane and a second surface defining a second plane, the package substrate having a cavity between the first plane and the second plane;

a first integrated circuit in the cavity; and

a second integrated circuit, coupled to the package substrate, outside the cavity.

17(**WITHDRAWN**). The package device of claim 16, wherein the substrate further comprises:

first pads on the first surface, second pads on the second surface, first bond fingers on the first surface and second bond fingers on the second surface.

18(**WITHDRAWN**). The package device of claim 17, wherein the first integrated circuit is electrically connected to the first pads and the second integrated circuit is electrically connected to second pads.

19(**WITHDRAWN**). The package device of claim 18, wherein the first pads are further characterized as being useful for receiving test probes for testing the first integrated circuit and the second pads are further characterized as being useful for receiving test probes for testing the second integrated circuit.

20(**WITHDRAWN**). The package device of claim 19, further comprising a conductive supporting member between the first integrated circuit and the second integrated circuit.

21(**WITHDRAWN**). A package device, comprising:

a package substrate having a first side and a second side;

first pads on the first side;

second pads on the second side;

a first integrated circuit mounted to the package substrate;

wherein the first pads and the second pads are further characterized as being useful for receiving test probes for testing.

22(**WITHDRAWN**). The package device of claim 21, further comprising a second integrated circuit mounted to the package substrate.

23(**WITHDRAWN**). The package device of claim 22, wherein:

the first integrated circuit is electrically connected to the first pads; and

the second integrated circuit is electrically connected to the second pads.

24(**WITHDRAWN**). The package device of claim 23, wherein the substrate is further characterized as having cavity and the first integrated circuit is further characterized as being in the cavity.

25(**WITHDRAWN**). The package device of claim 24, wherein the second integrated circuit is mounted to the substrate by adhesive die attach tape.

26(**WITHDRAWN**). The package device of claim 25, wherein the first integrated circuit is adjacent to the second integrated circuit.

27(**WITHDRAWN**). The package device of claim 26, further comprising a supporting member between the first integrated circuit and the second integrated circuit.

28(**ORIGINAL**). The method of claim 7, wherein the step of depositing the first portion of the encapsulating material comprises transfer molding the encapsulating material, and wherein the step of depositing a second portion of the encapsulating material comprises transfer molding the encapsulating material.

29(**ORIGINAL**). The method of claim 8, wherein the third integrated circuit is stacked at least partially overlying at least one of the first and second integrated circuits.

30(**NEW**). A method for forming a package device, comprising:

providing a package substrate having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane;

placing a first integrated circuit in the cavity;

placing a second integrated circuit adjacent to the first integrated circuit outside the cavity, such that a supporting member is interposed between the first integrated circuit and the second integrated circuit; and

depositing encapsulating material over the first integrated circuit and the second integrated circuit.

31(**NEW**). The method of claim 30, wherein die attach material is interposed between the first integrated circuit and the second integrated circuit.